FIG. 1
LOGIC CONES

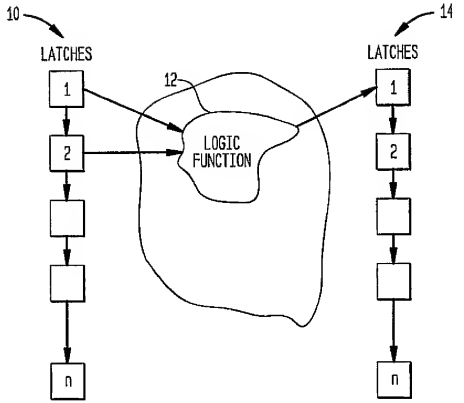
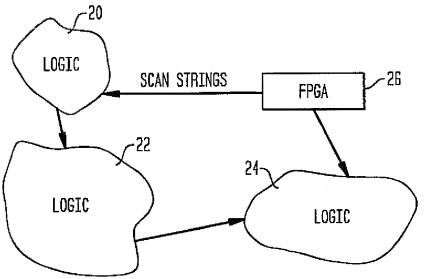


FIG. 2
STRUCTURE



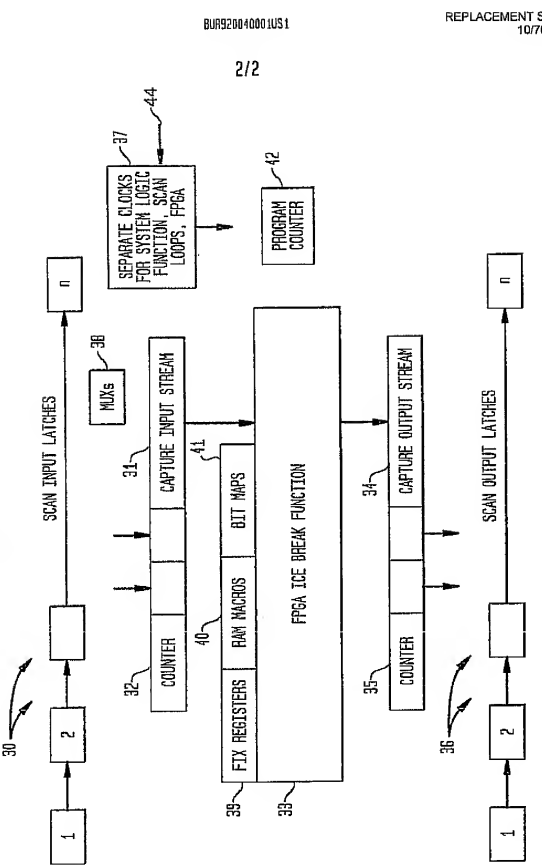


FIG. 3
FUNCTION TO FPGA
SCAN INPUT LATCHES
n
1
2
30
MUXs
38
SEPARATE CLOCKS FOR SYSTEM LOGIC FUNCTION, SCAN LOOPS, FPGA
37
44
PROGRAM COUNTER
42
CAPTURE INPUT STREAM
31
COUNTER
32
FIX REGISTERS
39
RAM MACROS
40
BIT MAPS
41
FPGA ICE BREAK FUNCTION
33
CAPTURE OUTPUT STREAM
34
COUNTER
35
36
SCAN OUTPUT LATCHES
n
1
2